ABSTRACT OF THE DISCLOSURE

A processing system for a charge coupled device (CCD) or CMOS imaging system includes a multi-mode, multiple current level, correlated double sample and variable gain (CDS/VGA) circuit for receiving data from a CCD system, subject to horizontal and vertical timing signals for the system which are locally generated by the processing system itself. The processing system particularly includes programmable timing circuitry for controlling the detection of pixel intensity values from elements of a two-dimensional pixel array, with a programmable low-frequency master vertical timing circuit driving a high-frequency horizontal timing circuit, wherein the vertical and horizontal timing signals are independently locally provided to the array from the analog processor actually sampling the array. The architecture of the processing system further includes a correlated double sampler, a black level clamp, and an A/D conversion module. The processing system includes a camera system for producing an imager signal, a correlated double sample (CDS) circuit for receiving data from an imager, a variable gain amplifier (VGA) having amplifiers of selectable current level to enable reduced data resolution, an analog-to-digital converter (ADC) having a selectable bit-width output and coupled to said VGA circuit, and a gain circuit coupled to said ADC. The single chip analog front end produces digitized CCD data in a bit formats corresponding to selected current level and data resolution. The VGA amplifier includes circuitry to enable selected data resolution levels respectively for still image capture and separate video display on another viewing screen.